REMARKS

Claims 1, 2, 4-9 15, 17 and 18-22 stand rejected as being anticipated by U.S. Pat. No. 6,502,156 (Sacker). Claims 3, 10-14, 16 and 24-25 stand rejected as being unpatentable over Sacker in view of U.S. Pat. No. 4,586,128 (DeWoskin). Claim 23 is rejected as being unpatentable over Sacker and DeWoskin and further in view of U.S. Patent No. 6,433,601 (Ganesan). Reconsideration of the rejections is solicited in view of the foregoing amendments and the following remarks.

Enclosed with this Amendment are copies of U.S. Pat. Nos. 5,812,858 and 5,835,733, which were cited in the IDS originally filed on 4 April 2001 but not considered by the Examiner. In view of this submission, applicant kindly requests consideration of the above-identified references.

As suggested in the Office Action, Claim 14 has been amended to correct linguistics inconsistencies therein, and, consequently, these grounds of rejection should be removed. Claims 1-9 have been cancelled.

The drawings have been amended as suggested in the Office Action to correct some drafting oversights, and accordingly applicant requests that the drawings objections be removed.

Regarding any rejection under 35 U.S.C. §103, it is respectfully noted that the test for patentability is whether there is some teaching or suggestion in the prior art references to support their use to reject the claimed invention. It is a basic tenet of patent law that the PTO is not permitted to ignore the results and advantages produced by claimed subject matter, of which the prior art is devoid, simply because the recited structure may be similar to that otherwise barren prior art. Further, when evaluating a claim for determining obviousness, all structural and operational interrelationships of the claim must be evaluated.

Applicant further notes that it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. The Court of Appeals Federal Circuit has previously stated that "[o]ne cannot use hindsight

reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention."

Claim 10 is directed to a method for hiding from a computer host, devices that share a common electrical bus. Claim 10 in part recites imparting a predefined time delay to a bus grant signal, wherein the time delay corresponds to a clocking cycle of a clock signal for the electrical bus. Claim 10 further recites propagating the bus grant signal to the controller upon completion of the clocking cycle and the signal indicative of the presence of the add-in card actually indicating the presence of the add-in card. These operational relationships allow propagating the bus grant signal synchronously with the bus clock signal for effecting the control rights of the processor over the controller. This avoids or reduces the possibility of potential race conditions that could result in a conflict between the host computer and the processor in connection with control rights over the controller. It is respectfully submitted that when considering the totality of claim 10 neither Sacker nor the secondary references, i.e., DeWoskin and Ganesan, singly or in combination, teach or suggest the foregoing operational relationships. Applicant recognizes that use of a bus grant signal and imparting a time delay to a signal *per se* is not new, however, applicant respectfully quotes former Chief Judge Markey of the Federal Circuit, "virtually all inventions are combinations and *every* invention is formed of old elements . . . Only God works from nothing. Man must work with old elements".

Claim 10 further recites non-intermittently masking a host device select signal in response to a signal indicative of the presence of an add-in card including a processor. By way of comparison, Sacker states that the IDSEL signal is used as a chip select signal during configuration cycles initiated by the host processor 12. However, the I/O processor 38 needs to hold off the host processor 12 by issuing retries until it has completed its own initialization. See Sacker col. 3, line 26 et. seq., line 55 et. seq. Thus, in Sacker there is a window of opportunity during such retries where the host processor may unintentionally assert control over the I/O device 26. The present invention advantageously avoids such a possibility since the host device is non-intermittently masked in

response to the signal indicative of the presence of the add-in card. Metaphorically speaking, Sacker's approach reflects a "hide-and-seek" type of approach during the configuration cycles, whereas the present invention non-intermittently masks the host device select signal. That is, without having to perform configuration retries. It is respectfully submitted that none of the secondary references, i.e., DeWoskin and Ganesan, singly or in combination, remedy the foregoing deficiency of Sacker.

In view of the foregoing considerations, it is respectfully submitted that Sacker, DeWoskin and Ganesan, singly or in combination, fail to render claim 10 unpatentable. Since each of the dependent claims from independent claim 10 includes the structural and/or operational relationships respectively recited in such independent claim, it is also respectfully submitted that such references, singly or in combination, also fail to obviate each of such dependent claims.

Claim 15 is directed to a circuit for hiding peer devices from a computer host. Claim 15 in part recites a hiding module configured to non-intermittently hide a second peer device from the host whenever a signal indicates the presence of a first device so that the first device controls the second device. Claim 15 further recites a delay device for imparting a predefined time delay to a bus grant signal, wherein the time delay corresponds to a clocking cycle of a clock signal for the electrical bus. Claim 15 further recites that the delay device is electrically coupled to propagate the bus grant signal to the second device upon completion of the clocking cycle and the signal indicative of the presence of the first device actually indicating the presence of the first device. These structure and/or operational relationships allow propagating the bus grant signal synchronously with the bus clock signal for effecting the control rights of the first device over the second device. This avoids or reduces the possibility of a potential race condition that could result in a conflict between the host computer and the first device in connection with control rights over the second device. It is respectfully submitted that when considering the totality of claim 15, neither Sacker nor the secondary references, i.e., DeWoskin and Ganesan, teach or suggest the foregoing structural and/or operational relationships. Since each of

the dependent claims from independent claim 15 includes the structural and/or operational relationships respectively recited in such independent claim, it is also respectfully submitted that such references, singly or in combination, also fail to obviate each of such dependent claims.

It is respectfully submitted that each of the claims pending in this application recites patentable subject matter and it is further submitted that such claims comply with all statutory requirements and thus each of such claims should be allowed.

The applicant appreciates the Examiner's efforts for conducting a thorough examination, and cordially invites the Examiner to call the undersigned attorney if there are any outstanding items that may be resolved via telephone conference.

Respectfully submitted,

Enrique J. Mora, Esquire
Registration No. 36,875
Beusse, Brownlee, Wolter, Mora & Maire, P.A.
390 North Orange Avenue, Suite 2500
Orlando, Florida 32801
Telephone: (407) 926-7705
Facsimile: (407) 926-7720

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I hereby certify that a true and correct copy of the above Amendment was furnished by First Class Mail to the Commissioner of Patents, MAIL STOP FEE AMENDMENT, P.O. Box 1450, Alexandria, VA 22313-1450 on this 31st day of March, 2004.

Grayce A. Lichtenberger